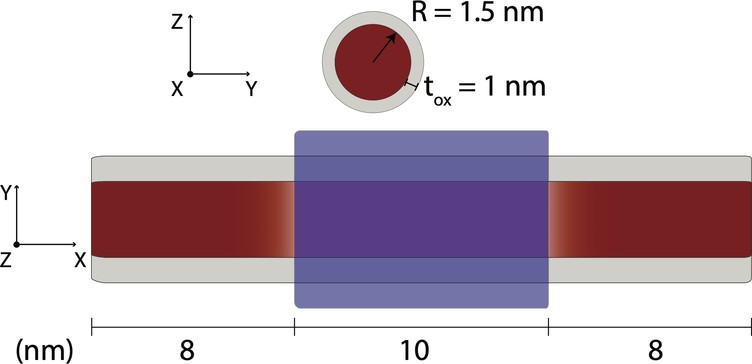
DEVICE SIMULATION (VLSI COURSE PROJECT)

### SIMULATED IN M\* SOFTWARE

Si-NWFET(Silicon nanowire FET)

**P.HARISH RAGAVENDER S20220020301**



## Si-NWFET(Silicon nanowire FET):

The schematic illustrates the device geometry:

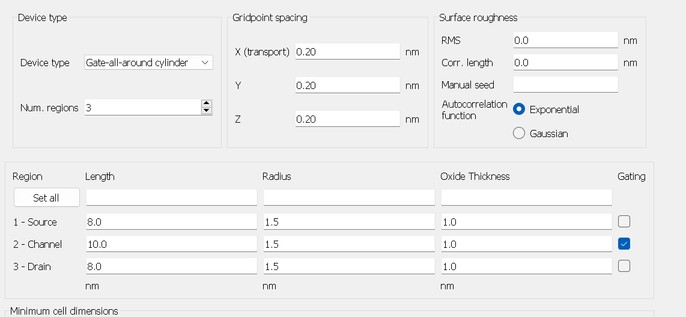
**Red**: Represents **silicon**.

**Gray**: Represents **silicon dioxide**. **Blue**: Represents the **gate electrode**.

**Different shades of red**: Indicate **variations in doping** levels across various device regions.

# INPUT PARAMETERS:

DEVICE PARAMETERS



THE DEVICE TYPE WE HAVE TAKEN IS **GATE ALL AROUND DEVICE** WITH

### CYLINDRICAL CROSS SECTION

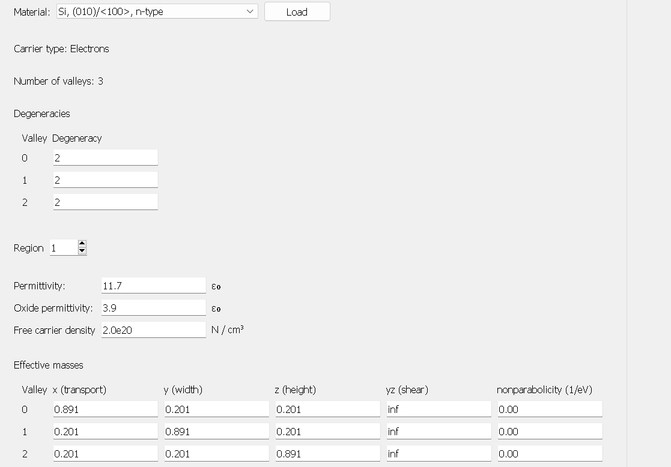
**NO. OF REGIONS** AS **3** AND **CHANNEL REGION** IS **GATED RADIUS** OF 1.5nm

**OXIDE THICKNESS** OF 1nm **CHANNEL LENGTH** OF 10nm **SOURCE/DRAIN REGION** OF 8nm **NO SURFACE ROUGHNESS**

### GRID POINT SPACING FOR X (TRANSPORT),Y,Z IS 0.20nm

**AUTOCORRELATION FUNCTION** IS EXPONENTIAL

MATERIAL PARAMETERS



THE MATERIAL WE HAVE SELECTED IS **Si, (010)/<100>,n-type** WITH CARRIER TYPE AS **ELECTRONS**

### NO. OF VALLEYS: 3

**VALLEY DEGENERACY:** 2

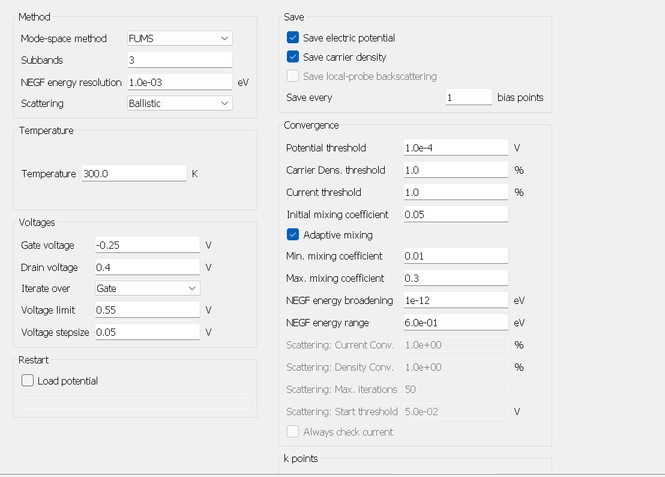
**PERMITTIVITY:** 11.7

### OXIDE PERMITTIVITY: 3.9

FOR **SOURCE** AND **DRAIN REGION** SET **2.0e20 N/CM^3** - CARRIER DENSITY FOR **CHANNEL REGION**

SET **0 N/CM^3** - CARRIER DENSITY

CONTROL PARAMETERS



**MODE:** FAST UNCOUPLED MODE-SPACE METHOD (FUMS)

### SUBBANDS: 3

**NEGF ENEREGY RESOLUTION:** 1.0e-03 ev **SCATTERING:** BALLISTIC SCATTERING **TEMPERATURE:** 300K(ROOM TEMPERATURE) **DRAIN VOLTAGE:** 0.40V

**GATE VOLTAGE:** -0.25V (INITIAL GATE BIAS) **VOLTAGE LIMIT:** 0.55V WITH **STEP SIZE** OF 0.05V **POTENTIAL THRESHOLD:** 1.0e-4

### CURRENT DENSITY AND CURRENT THRESHOLD: 1%

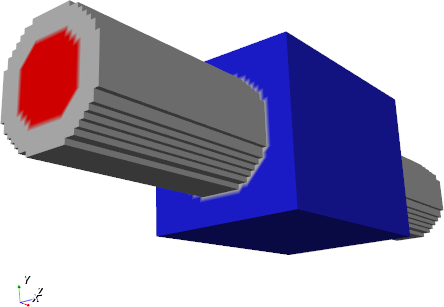
**INITIAL MIXING COEFFICIENT:** 0.05 **ENABLE ADAPTIVE MIXING: MINIMUM COEFFICIENT:** 0.01

**MAXIMUM COEFFICIENT:** 0.3

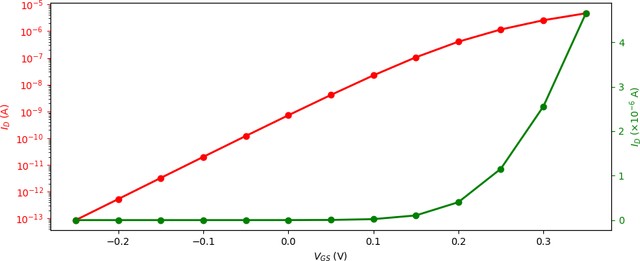
# OUTPUT INFERENCE:

THE BELOW SHOWN FIGURE IS THE **3D GEOMETRY** OF **Si-NWFET(Silicon**

## nanowire FET)



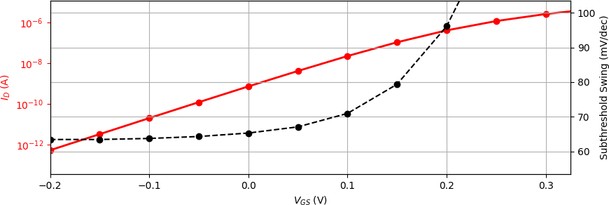
**DEVICE TRANSFER CHARACTERISTICS (I-V)**



THE DEVICE TRANSFER CHARACTERISTICS GRAPH TYPICALLY PLOTS THE **INPUT PARAMETER (VGS)** ON THE X-AXIS AGAINST THE **OUTPUT PARAMETER (ID)** ON THE Y-AXIS.

RED DENOTES SEMILOGARITHMIC (LEFT, VERTICAL AXIS) GREEN DENOTES LINEAR PLOTS (RIGHT, VERTICAL AXIS)

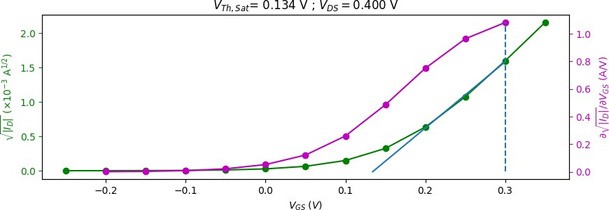
## SUBTHRESHOLD SWING



SUBTHRESHOLD SWING **DEPENDENCE WITH GATE BIAS**

DEVICE EXHIBITS VALUE **BELOW 70mV/dec** FOR **GATE VOLTAGES BELOW 0.1V**

## THRESHOLD VOLTAGE



DETERMINING THE THRESHOLD VOLTAGE (Vth)

GRAPH THAT PLOTS THE **RELATIONSHIP BETWEEN GATE VOLTAGE (VGS)** AND **DEVICE CURRENT(ID)**

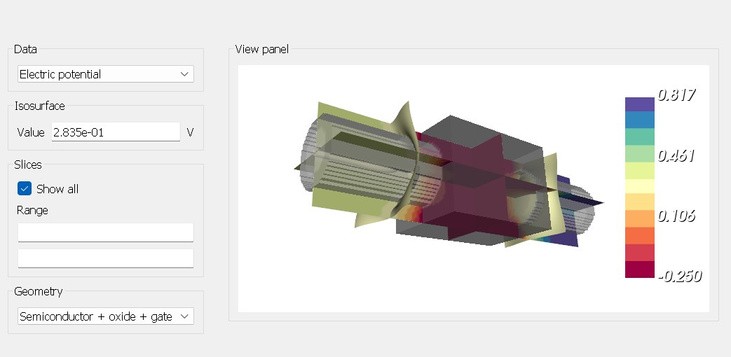
BLUE LINE IS SHOWED FOR CALCULATING THE SLOPE OF THE GREEN CURVE (STEEPNESS) THE GREEN CURVE REPRESENTS HOW CURRENT CHANGES WITH GATE VOLTAGE

**MAGENTA CURVE** REPRESENTS **THE DERIVATIVE OF THE CURRENT**, THIS SHOWS **HOW FAST CURRENT CHANGES AS GATE VOLTAGE INCREASES**

**A VERTICAL DASHED LINE** MARKS THE POINT WHERE **MAGENTA CURVE REACHES** ITS **HIGHEST VALUE** (AT THAT POINT DEVICE IS **MOST RESPONSIVE TO CHANGES IN GATE VOLTAGE)**

THE THRESHOLD VOLTAGE (Vth) IS DETERMINED ,WHERE THE **BLUE LINE CROSSES THE ORIGIN,**AT THAT POINT **DEVICE FIRST BEGINS TO CONDUCT CURRENT** THAT IS CALLED **THRESHOLD VOLTAGE**

## 3D VISUALISATION (ELECTRIC POTENTIAL)



**ELECTRIC POTENTIAL** DETERMINES HOW **ELECTRIC CHARGES WILL MOVE WITHIN THE DEVICE** AND **REGIONS WITH HIGHER ELECTRIC POTENTIAL** ARE TYPICALLY

INFLUENCED BY **APPLIED VOLTAGE, MATERIAL PROPERTIES** AND **DEVICE GEOMETRY**

HIGHER ELECTRIC POTENTIAL NEAR ELECTRODES WHERE VOLTAGE IS APPLIED,

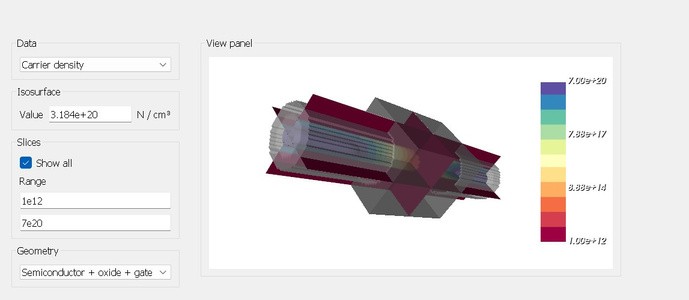
AND IN **GATE CONTROLLED REGIONS**

THIS SHOWS THE ELECTRIC POTENTIAL IN DIFFERENT REGIONS WITH **DIFFERENT COLOUR SHADES IN 3D VISUALISATION**

THIS SHOWS DIFFERENT **SLICES** ALONG **X ,Y Z AXES**

THIS GEOMETRY INCLUDES **SEMICONDUCTOR+OXIDE+GATE**

## 3D VISUALISATION (CARRIER DENSITY)



SAME AS ELECTRIC POTENTIAL ,IT SHOWS CARRIER DENSITY

CARRIER DENSITY REFERS TO **CONCENTRATION OF CHARGE CARRIERS** [**ELECTRONS OR HOLES**] IN A SEMICONDUCTOR DEVICE

REGION WITH **HIGHER CARRIER DENSITY** DEPEND ON **MATERIAL PROPERTIES, DOPING LEVELS** AND **APPLIED VOLTAGE**

**DIFFERENT SHADES OF COLOUR** SHOWS LEVEL OF CONCENTRATION OF CARRIER DENSITY

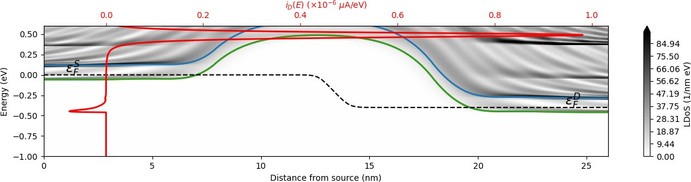
**HIGHER CARRIER DENSITY** OCCURS IN **HEAVILY DOPED REGIONS (SOURCE/DRAIN)** UNDER **STRONG INVERSION (GATE VOLTAGE GREATER THAN Vth)** FORMING A **STRONG CONDUCTIVE CHANNEL** ALLOWING **LARGE CURRENT TO FLOW** TYPICALLY FUNCTIONING AS **SWITCH** IN **ON STATE**

**LOWER CARRIER DENSITY** OCCURS IN **LIGHTLY DOPED REGION** AND SEEN IN

DEPLETION REGION

**IN REVERSE BIAS** MAKING **DEPLETION REGION WIDER** FORMING **BARRIER** SO LOWER CARRIER DESNITY

## 2D VISUALISATION



THIS 2D VISUALISATION INCLUDES

LDOS REPRESENTS THE NUMBER OF ELECTRONIC STATES AVAILABLE PER UNIT

ENERGY AND UNIT VOLUME AT A SPECIFIC POSITION WITHIN THE DEVICE

**GRAY AREAS:** REPRESENT REGIONS WITH LOWER LDOS **(FEWER AVAILABLE STATES AT THAT ENERGY AND POSITION)**

**BLACK AREAS:** REPRESENT REGIONS WITH HIGHER LDOS **(MORE DENSELY PACKED ELECTRONIC STATES)**

BOTTOM AXES SHOWS THE DISTANCE FROM SOURCE (IN nm) TOP AXES SHOWS VARIATION IN CURRENT

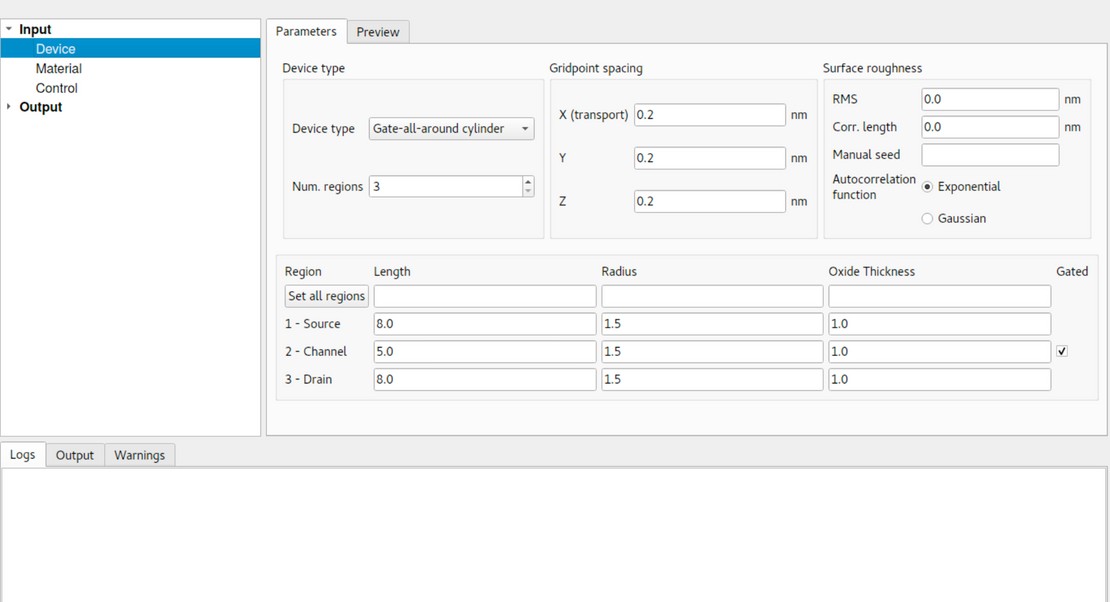
**ENERGY VALLEYS** (BLUE AND GREEN LINES) ILLUSTRATE THE **DIFFERENT ENERGY**

STATES AVAILABLE FOR ELECTRONS

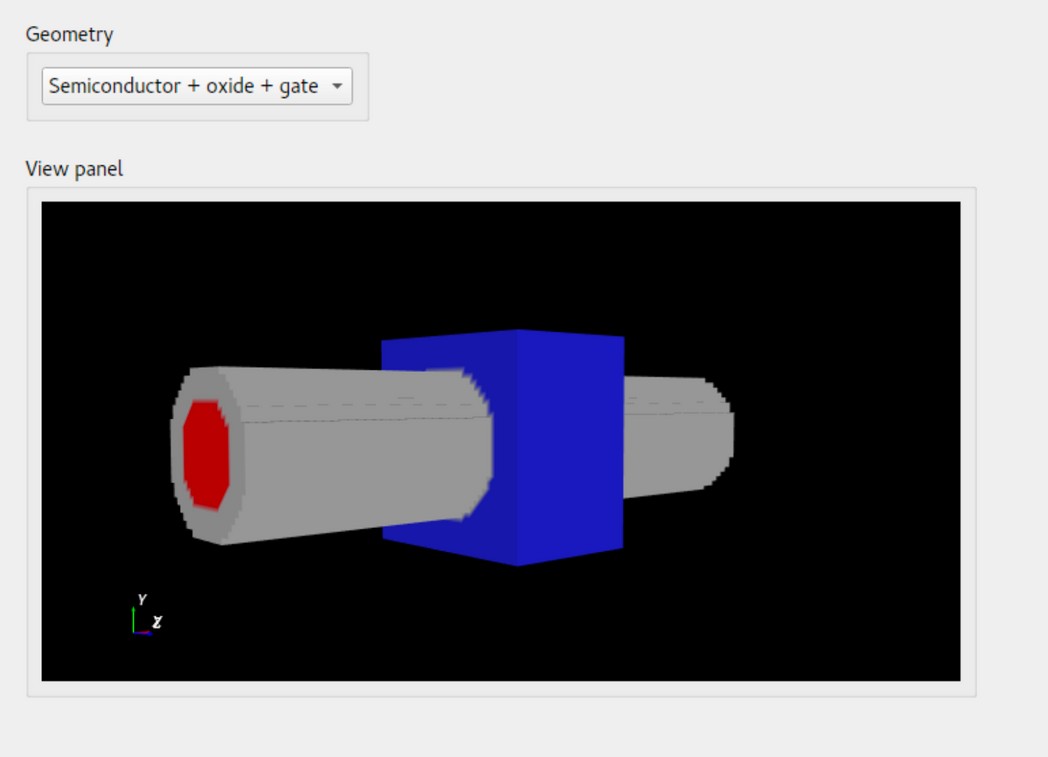
TUNNELING MEANS CHARGE CARRIERS (ELECTRONS) TO PASS THROUGH BARRIERS

**SHORTER CHANNEL LENGTH** WILL HAVE **STRONG SOURCE TO DRAIN TUNNELLING CONTRIBUTION** WILL RESULT IN **INCREASED LEAKAGE CURRENT** WHEN TRANSISTOR IS SUPPOSED TO BE **OFF** IT CAN LEAD TO **HIGHER POWER CONSUMPTION REDUCE DEVICE PERFORMANCE**

## REDUCING THE CHANNEL LENGTH TO 5nm (SO TECHNOLOGY NODE IS 5nm)

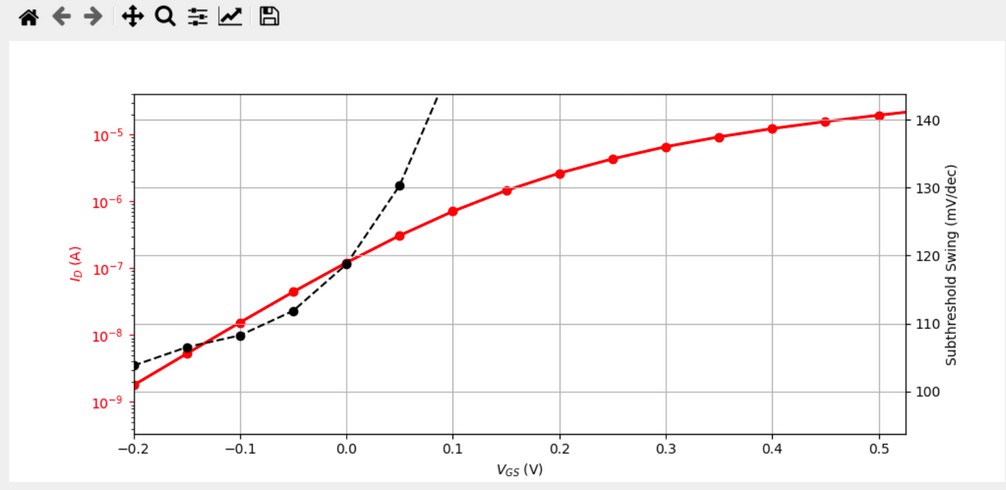


**3D GEOMETRY (REDUCED CHANNEL LENGTH)**



YOU CAN CLEARLY SEE THE **REDUCED CHANNEL LENGTH IN THIS 3D GEOMETRY** WHEN **COMPARE TO THE PREVIOUS 3D GEOMETRY(10nm)** MAKING THE DEVICE TO HAVE **REDUCED SWITCHING TIME** ,**INCREASED DRIVE CURRENT** AND **INCREASED SHORT CHANNEL EFFECT**

## SUBTHRESHOLD SWING (REDUCED CHANNEL LENGTH)

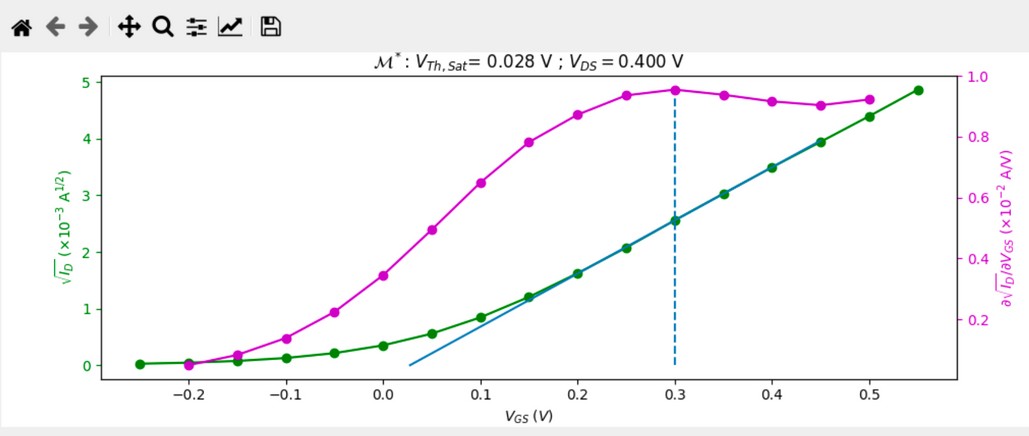


REDUCING THE DEVICE'S GATE LENGTH RESULTS IN AN **INCREASE OF THE SUBTHRESHOLD SWING**

AND AT **Vgs=-0.1** AND **BELOW** IT IS **110mV/dec**

AFTER IT IS **EXPONENTIALLY INCREASING**

## THRESHOLD VOLTAGE (REDUCED CHANNEL LENGTH)

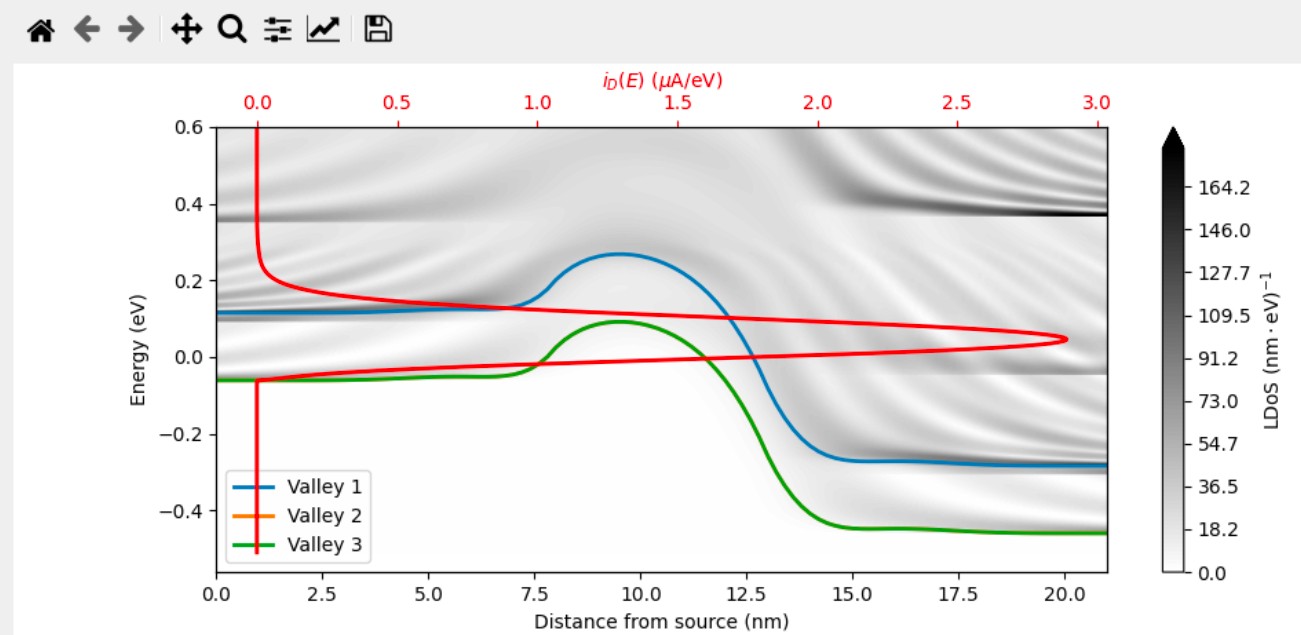


REDUCING THE DEVICE'S GATE LENGTH RESULTS IN A **SHIFT OF THE THRESHOLD VOLTAGE TOWARDS A LOWER GATE BIAS** DUE TO SHORT-CHANNEL EFFECTS

PREVIOUSLY **Vth IS AT 0.134V** AT **10nm technology node**

REDUCING THE CHANNEL LENGTH MAKES **Vth AT 0.028V(5nm)**

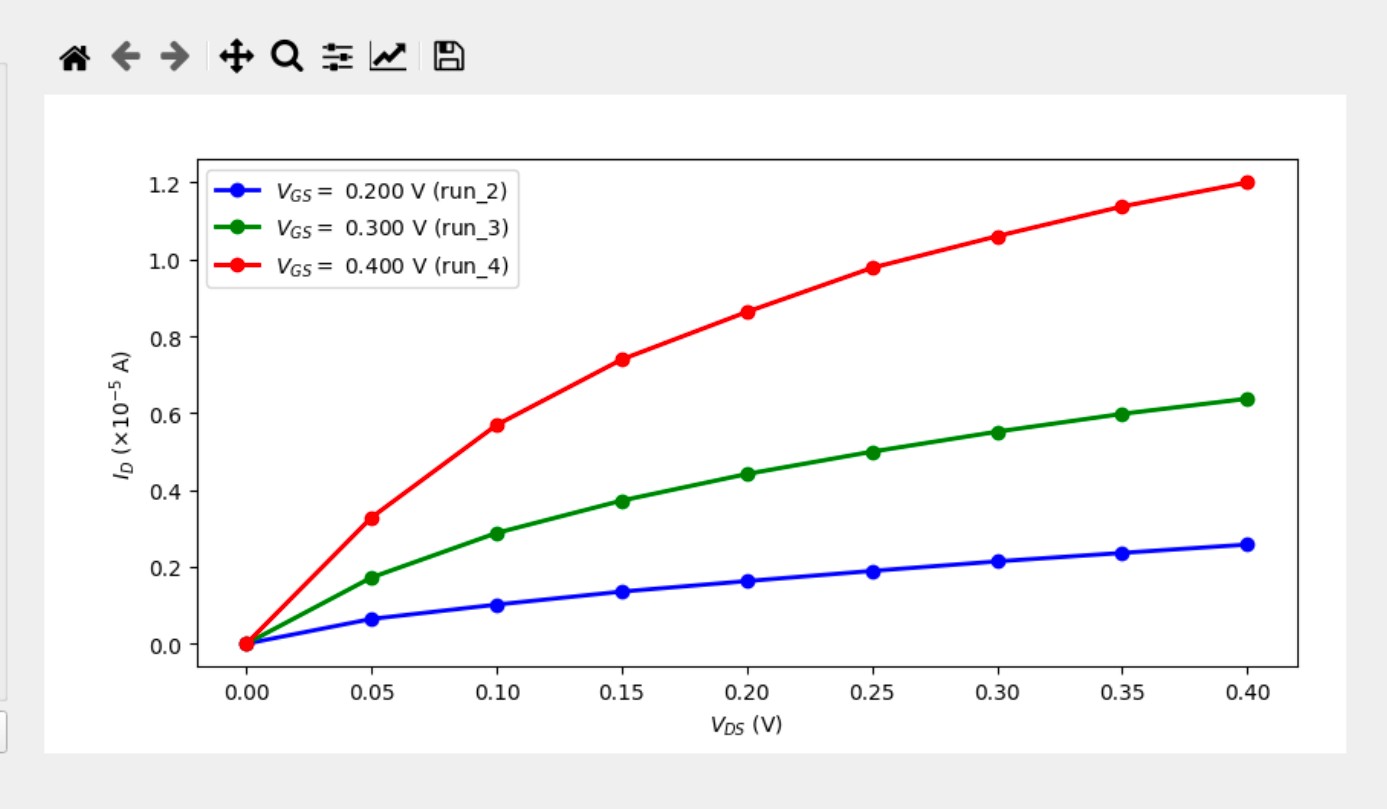
## 2D VISUALISATION FOR SHORTER CHANNEL LENGTH (5nm) FOR ON CURRENT



A SHORTER CHANNEL LENGTH **INCREASES THE TUNNELLING CURRENT BETWEEN THE SOURCE AND DRAIN** DUE TO HIGHER ELECTRIC FIELDS, ENHANCED SHORT-CHANNEL EFFECTS

**STRONG** SOURCE TO DRAIN TUNNELLING

## DRAIN SWEEP CHARACTERISTICS OF ID CURRENT AND VDS VOLTAGE FOR DIFFERENT VGS (0.2,0.3,0.4)



**THE DRAIN SWEEP CHARACTERISTICS** OF **(ID)CURRENT** AND **(VDS)VOLTAGE** FOR DIFFERENT **(VGS)VALUES (0.2, 0.3, 0.4)** SHOW THAT AS **(VGS) INCREASES**, THE DRAIN CURRENT **(ID) INCREASES**, INDICATING BETTER CONDUCTION. **THE (ID) CURRENT REMAINS CONSTANT BEYOND A CERTAIN (VDS) (SATURATION REGION)**, WITH THE **TRANSITION POINT OCCURRING SOONER FOR HIGHER (VGS)VALUES**

## CONCLUSION:

I HAVE INFERRED KEY ASPECTS OF **3D GEOMETRY** RELATED TO **DEVICE TRANSFER CHARACTERISTICS, SUB THRESHOLD SWING AND THRESHOLD VOLTAGE THROUGH 2 D , 3D VISUALISATION OF ELECTRIC POTENTIAL AND CARRIER DENSITY**

THIS APPROACH ENHANCES THE **UNDERSTANDING OF DEVICE PERFORMANCE IN SEMICONDUCTOR PHYSICS**